AMENDMENTS TO THE CLAIMS

1. (Currently amended) A partial product bit generator circuit for use in performing multiplication to generate a product of a multiplicand and a multiplier, the multiplicand being represented by a digital signal having a plurality of bits, the multiplier being represented by a digital signal having a plurality of bits, the partial product bit generator circuit receiving a group of the multiplicand bits and a group of the multiplier bits and providing a partial product bit in response thereto, wherein the partial product bit generator circuit comprises less than six levels of combinatorial logic and further comprises:

a first circuit, responsive to a group of the multiplicand bits and a first subset of a group of the multiplier bits, to output at least three digital signals;

a second circuit, responsive to a second subset of the group of multiplier bits, to output at least three select signals, each of the at least three select signals being associated with a respective one of the at least three digital signals, only one of the at least three select signals having a logic state that is asserted; and

a third circuit, to output a partial product bit in response to the digital signal that is associated with the select signal having the asserted logic state.

2. (Canceled)

3. (Currently amended) The partial product bit generator circuit of claim ~~2~~1 wherein the third circuit comprises less than four levels of combinatorial logic.

4. (Currently amended) The partial product bit generator circuit of claim ~~2~~1 wherein the third circuit comprises only one level of combinatorial logic.

5. (Currently amended) A partial product bit generator circuit as in any of claims [[2-4]]3 or 4 wherein the first circuit and the second circuit each comprise only two levels of combinatorial logic.

6. (Original) The partial product bit generator circuit of claim 1 wherein the partial product bit generator comprises less than five levels of combinatorial logic.

7. (Original) The partial product bit generator circuit of claim 1 wherein the partial product bit generator comprises less than four levels of combinatorial logic.

8. (Original) The partial product bit generator circuit of claim 1 wherein the partial product bit generator comprises exactly three levels of combinatorial logic.

9. (Original) The partial product bit generator circuit of claim 1 wherein a longest delay path through the partial product bit generator circuit is substantially equivalent to an XOR gate and a three input pass transistor multiplexer.

10. (Original) A method for use in performing multiplication to generate a product of a multiplicand and a multiplier, the multiplicand being represented by a digital signal having a plurality of bits, the multiplier being represented by a digital signal having a plurality of bits, the method comprising:

receiving a group of the multiplicand bits;

receiving a group of the multiplier bits;

generating a partial product bit signal in response to the group of multiplicand bits and the group of multiplier bits using less than six levels of combinatorial logic, wherein generating comprises:

generating at least three digital signals in response to the group of multiplicand bits and a first subset of the group of multiplier bits;

generating at least three select signals in response to a second subset of the group of multiplier bits, each of the at least three select signals being associated with a respective one of the at least three digital signals, only one of the select signals having a logic state that is asserted; and

generating a partial product bit in response to the digital signal associated with the select signal having the asserted logic state.

11. (Canceled)

12. (Original) The method of claim 10 wherein generating comprises generating a partial product bit signal in response to the group of multiplicand bits and the group of multiplier bits using less than five levels of combinatorial logic.

13. (Original) The method of claim 10 wherein generating comprises generating a partial product bit signal in response to the group of multiplicand bits and the group of multiplier bits using less than four levels of combinatorial logic.

14. (Original) The method of claim 10 wherein generating comprises generating a partial product bit signal in response to the group of multiplicand bits and the group of multiplier bits using exactly three levels of combinatorial logic.

15. (Canceled)

17. (Original) A method for use in performing multiplication to generate a product of a multiplicand and a multiplier, the multiplicand being represented by a plurality of bits, the multiplier being represented by a plurality of bits, the method comprising:

receiving a group of the multiplicand bits;

receiving a group of the multiplier bits;

generating at least three digital signals in response to the group of multiplicand bits and a first subset of the group of multiplier bits;

generating at least three select signals in response to a second subset of the group of multiplier bits, each of the at least three select signals being associated with a respective one of the at least three digital signals, only one of the select signals having a logic state that is asserted; and

generating a partial product bit in response to the digital signal associated with the select signal having the asserted logic state.

18. (Original) The method of claim 17 wherein the generating of the at least three digital signals is performed concurrent with the generating of the set of at least three select signals.

19. (Original) The method of claim 17 wherein the first subset of the group of multiplier bits is not equal to the second subset of the group of multiplier bits.

20. (Original) The method of claim 19 wherein the first subset of the group of multiplier bits includes only a most significant bit of the group of multiplier bits.

21. (Original) The method of claim 19 wherein the second subset of the group of multiplier bits includes all of the group of multiplier bits except for a most significant bit of the group of multiplier bits.

22. (Original) The method of claim 20 wherein the second subset of the group of multiplier bits includes all of the group of multiplier bits except for a most significant bit of the group of multiplier bits.

23. (Original) The method of claim 22 wherein the group of multiplier bits comprises exactly three multiplier bits.

24. (Original) The method of claim 23 wherein the group of multiplicand bits comprises exactly two bits, the at least three digital signals comprise exactly three digital signals, and the at least three select signals comprise exactly three select signals.

25. (Original) The method of claim 17 wherein generating a partial product bit comprises:

selecting the digital signal that is associated with the select signal having the asserted logic state; and

generating the partial product bit in response to the selected digital signal.

26. (Original) The method of claim 25 wherein generating the partial product bit in response to the selected digital signal comprises generating a partial product bit having a logic state that is equal to that of the selected digital signal.

27. (Original) The method of claim 17 wherein the group of multiplier bits comprises exactly three multiplier bits, b_{j+1}, b_j, b_{j-1}, the group of multiplicand bits comprises exactly two bits, a_i, a_{i-1}, the at least three digital signals comprise exactly three digital signals, $aa_{1,-1}$, aa_2, aa_{-2}, and the at least three select signals comprise exactly three select signals, $s_{1,-1}$, s_2, s_{-2}, and wherein the digital signal $aa_{1,-1}$ has a logic state equal to the logic state of a_i XOR b_{j+1}, the digital signal aa_2 has a logic state equal to the logic state of a_{i-1} NOT (b_{j+1}), and the digital signal aa_{-2} has a logic state equal to the logic state of NOT(a_{i-1}) b_{j+1}.

28. (Original) The method of claim 27 wherein the select signal $s_{1,-1}$ has a logic state equal to the logic state of b_j XOR b_{j-1}, the select signal s_2 has a logic state equal to the logic state of b_j b_{j-1}, and the select signal s_{-2} has a logic state equal to the logic state of NOT(b_j) NOT (b_{j-1}).

29. (Original) The method of claim 28 wherein the partial product bit has a logic state equal to the logic state of $s_{1,-1}\, aa_{1,-1} + s_2\, aa_2 + s_{-2}\, aa_{-2}$.

30. (Original) Apparatus for use in performing multiplication to generate a product of a multiplicand and a multiplier, the multiplicand being represented by a digital signal having a plurality of bits, the multiplier being represented by a digital signal having a plurality of bits, the apparatus comprising:

a first circuit, responsive to a group of the multiplicand bits and a first subset of a group of the multiplier bits, to output at least three digital signals;

a second circuit, responsive to a second subset of the group of multiplier bits, to output at least three select signals, each of the at least three select signals being associated with a respective one of the at least three digital signals, only one of the at least three select signals having a logic state that is asserted; and

a third circuit, to output a partial product bit in response to the digital signal that is associated with the select signal having the asserted logic state.

31. (Original) The apparatus of claim 30 wherein the first subset of the group of multiplier bits is not equal to the second subset of the group of multiplier bits.

32. (Original) The apparatus of claim 31 wherein the group of multiplier bits comprises exactly three bits, the first subset of the group of multiplier bits includes only a most significant bit of the group of multiplier bits, and the second subset of the group of multiplier bits includes all of the group of multiplier bits except for a most significant bit of the group of multiplier bits.

33. (Original) The apparatus of claim 30 wherein the group of multiplier bits comprises exactly three multiplier bits, b_{j+1}, b_j, b_{j-1}, the group of multiplicand bits comprises exactly two bits, a_i, a_{i-1}, the at least three digital signals comprise exactly three digital signals, $aa_{1,-1}$, aa_2, aa_{-2}, and the at least three select signals comprise exactly three select signals, $s_{1,-1}$, s_2, s_{-2}, the digital signal $aa_{1,-1}$ has a logic state equal to the logic state of a_i XOR b_{j+1}, the digital signal aa_2 has a logic state equal to the logic state of a_{i-1}NOT(b_{j+1}), and the digital signal aa_{-2} has a logic state equal to the logic state of NOT(a_{i-1}) b_{j+1}, the select signal $s_{1,-1}$ has a logic state equal to the logic state of b_j XOR b_{j-1}, the select signal s_2 has a logic state equal to the logic state of b_j b_{j-1}, the select signal s_{-2} has a logic state equal to the logic state of NOT(b_j) NOT (b_{j-1}), and the partial product bit has a logic state equal to the logic state of $s_{1,-1}\, aa_{1,-1} + s_2\, aa_2 + s_{-2}\, aa_{-2}$.

34. (Original) The apparatus of claim 30 wherein the first circuit and the second circuit have substantially the same propagation delay as one another.

35. (Original) The apparatus of claim 30 wherein the longest logic path through the first circuit and the second circuit is substantially equal to an XOR gate.

36. (Original) The apparatus of claim 30 wherein the third circuit comprises a pass-transistor multiplexer, responsive to the at least three select signals, to output the digital signal that is associated with the select signal having the asserted logic state.

37. (Original) A partial product bit generator circuit for use in performing multiplication to generate a product of a multiplicand and a multiplier, the multiplicand being represented by a digital signal having a plurality of bits, the multiplier being represented by a digital signal having a plurality of bits, the partial product bit generator circuit receiving a group of the multiplicand bits and a group of the multiplier bits, the partial product bit generator circuit comprising:

a first circuit, responsive to the group of multiplicand bits and a first subset of the group of multiplier bits, to output a first set of output signals;

a second circuit, responsive to a second subset of the group of multiplier bits to output a second set of output signals, the second subset of the group of multiplier bits being disjoint from the first subset of the group of multiplier bits ; and

a third circuit, responsive to the first set of output signals and the second set of output signals to output a partial product bit signal.

38. (Original) The partial product bit generator circuit of claim 37 wherein the third circuit is responsive only to the first set of output signals and the second set of output signals.

39. (Original) The partial product bit generator circuit of claim 37 wherein the first circuit and the second circuit operate concurrent with one another.

40. (Original) The partial product bit generator circuit of claim 38 wherein the first circuit and the second circuit operate concurrent with one another.

41. (Original) The partial product bit generator circuit of claim 37 wherein the first circuit and the second circuit have about the same propagation delay.

42. (Original) The partial product bit generator circuit of claim 38 wherein the first circuit and the second circuit have about the same propagation delay.

43. (Original) The partial product bit generator circuit of claim 40 wherein the first circuit and the second circuit have about the same propagation delay.

44. (Original) A method for use in performing multiplication to generate a product of a multiplicand and a multiplier, the multiplicand being represented by a digital signal having a plurality of bits, the multiplier being represented by a digital signal having a plurality of bits, the method comprising:

receiving a group of the multiplicand bits;

receiving a group of the multiplier bits;

generating a first set of output signals in response to the group of multiplicand bits and a first subset of the group of multiplier bits;

generating a second set of output signals in response to a second subset of the group of multiplier bits, the second subset of the group of multiplier bits being disjoint from the first subset of the group of multiplier bits ; and

generating a partial product bit signal in response to the first set of output signals and the second set of output signals.

45. (Original) An apparatus for use in performing multiplication to generate a product of a multiplicand and a multiplier, the multiplicand being represented by a plurality of bits, the multiplier being represented by a plurality of bits, the method comprising:

means for generating at least three digital signals in response to a group of the multiplicand bits and a first subset of a group of multiplier bits;

means for generating at least three select signals in response to a second subset of the group of multiplier bits, each of the at least three select signals being associated with a respective one of the at least three digital signals, only one of the select signals having a logic state that is asserted; and

means for generating a partial product bit in response to the digital signal associated with the select signal having the asserted logic state.

46. (Original) A partial product bit generator for use in performing multiplication to generate a product of a multiplicand and a multiplier, the multiplicand being represented by a digital signal having a plurality of bits, the multiplier being represented by a digital signal having a plurality of bits, the partial product bit generator circuit receiving a group of the multiplicand bits and a group of the multiplier bits, the partial product bit generator circuit comprising:

means for generating a first set of output signals in response to the group of multiplicand bits and a first subset of the group of multiplier bits;

means for generating a second set of output signals in response to a second subset of the group of multiplier bits, the second subset of the group of multiplier bits being disjoint from the first subset of the group of multiplier bits; and

means for generating a partial product bit signal in response to the first set of output signals and the second set of output signals.

47. (Original) A partial product bit generator that receives three multiplier bits, b_{j+1}, b_j, b_{j-1}, and two multiplicand bits, a_i, a_{i-1}, and outputs a partial product bit, wherein a longest delay path through the partial product bit generator circuit is substantially equivalent to an XOR gate and a three input pass transistor multiplexer.